FUJITSU SEMICONDUCTOR
DATA SHEET

DS704-00011-0v01-E

CMOS

F²MC-16FX MB96690 Series

MB96F696*

„ DESCRIPTION

MB96690 series is based on FUJITSU's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products.
16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

*: These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

PRELIMINARY

For the information for microcontroller supports, see the following website.

http://edevice.fujitsu.com/micom/en-support/

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2011.7

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal

z Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 × 8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture
- Start delay

z Stepper Motor Controller

- Stepper Motor Controller with integrated high current output drivers
- Four high current outputs for each channel
- Two synchronized 8/10-bit PWMs per channel
- Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock
- Dedicated power supply for high current output drivers

z LCD Controller

- LCD controller with up to 4 COM × 36SEG
- Internal or external voltage generation
- Duty cycle: Selectable from options: 1/2, 1/3 and 1/4
- Fixed 1/3 bias
- Programmable frame period
- Clock source selectable from four options (main clock, peripheral clock, subclock or RC oscillator clock)
-

External Interrupts

- Edge or Level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

z Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

z I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I^2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GP-IO-pin (either Automotive or CMOS-Schmitt trigger)
- Bit-wise programmable pull-up resistor

z Built-in OCD (On Chip Debugger)

- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - Software break: 4096 points
- Event function
  - Code event: 6 points (shared with hardware break)
  - Data event: 6 points
  - Event sequencer: 2 levels
- Execution time measurement function
- Trace function: 42 branches
- Security function

z Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase

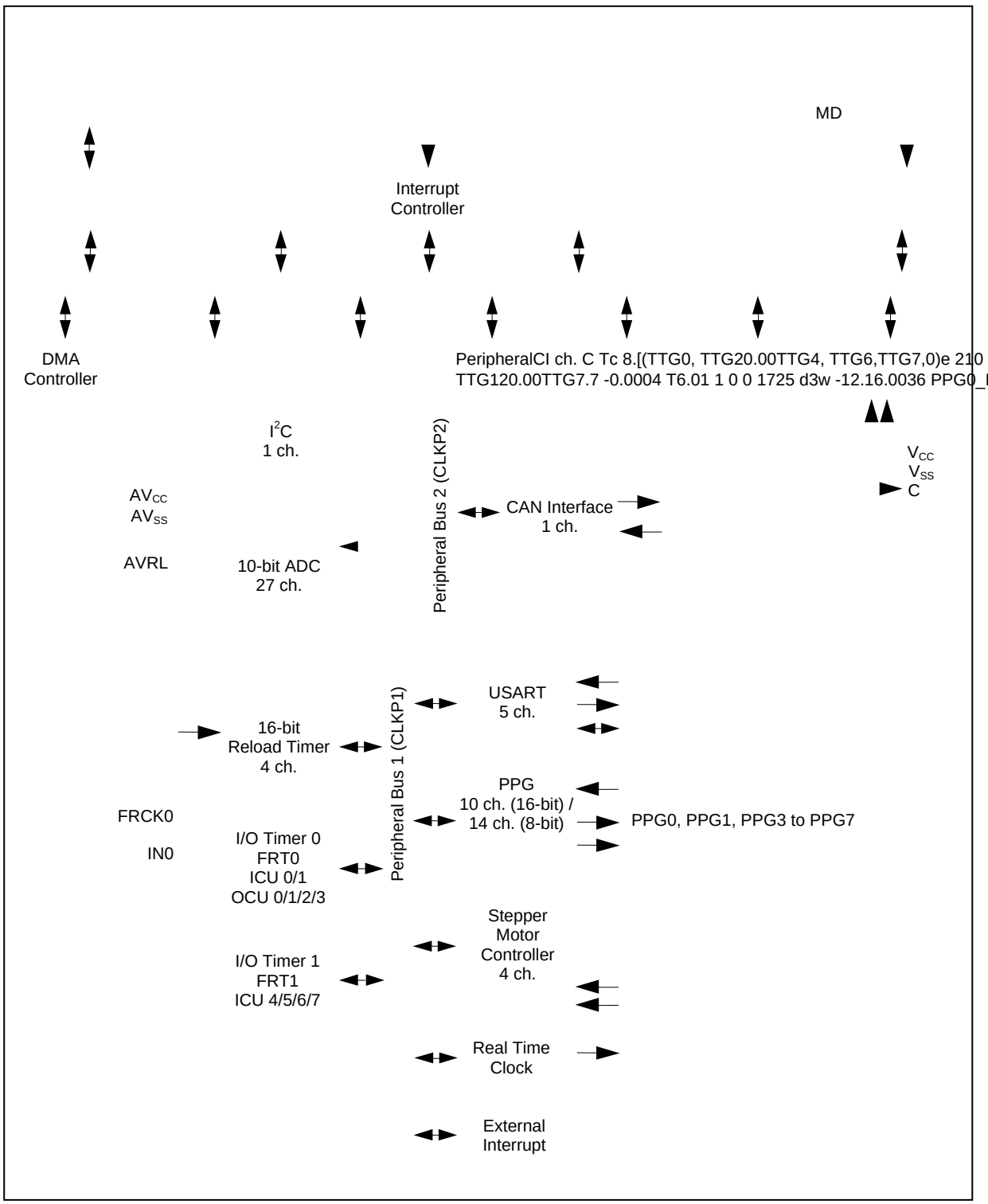
PRODUCT LINEUP

Features		MB96F69x	Remark
Product type		Flash product	
Subclock		Subclock can be set by software	
Dual Operation Flash memory	RAM		
256.5KB + 32KB	16KB	MB96F696	
Package		LQFP-100 FPT-100P-M20	
DMA		4ch	
USART		5ch	LIN-USART 0/1/2/4/5
	with automatic LIN-Header transmisstion/reception	2ch	LIN-USART 0/1
	with 16 byte RX- and TX-FIFO		
I^2C		1ch	I^2C 0
10-bit A/D Converter		27ch	AN 2 to 4/6 to 8/10 to 12/ 14 to 31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	Yes	
16-bit Reload Timer (RLT)		5ch	RLT 0/1/2/3/6 Only RLT6 can be used as PPG clock source.
16-bit Free-Running Timer (FRT)		2ch	FRT 0/1
16-bit Input Capture Unit (ICU)		6ch (5 channels for LIN-USART)	ICU 0/1/4/5/6/7 ICU 0/1/4/5/6 for LIN-USART
16-bit Output Compare Unit (OCU)		4ch	OCU 0 to 3
8/16-bit Programmable Pulse Generator (PPG)		10ch (16-bit) / 14ch (8-bit)	PPG 0 to 7/14/15
	with Timing point capture	Yes	
	with Start delay	Yes	
	with Ramp	No	
CAN Interface		1ch	CAN 0 32 Message Buffers
Stepping Motor Controller (SMC)		4ch	SMC 0/1/2/4
External Interrupts (INTerrupt)		16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)		1ch	
Sound generator (SG)		2ch	SG 0/1
LCD Controller		4 COM × 36 SEG	COM 0 to 3 SEG 0 to 4/7/11 to 28/30/33/36 to 45
Real Time Clock (RTC)		1ch	
I/O Ports		77 (Dual clock mode) 79 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Reset		Yes	Low voltage reset can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Notes: ・All signals of the peripheral function in each product cannot be allocated by limiti

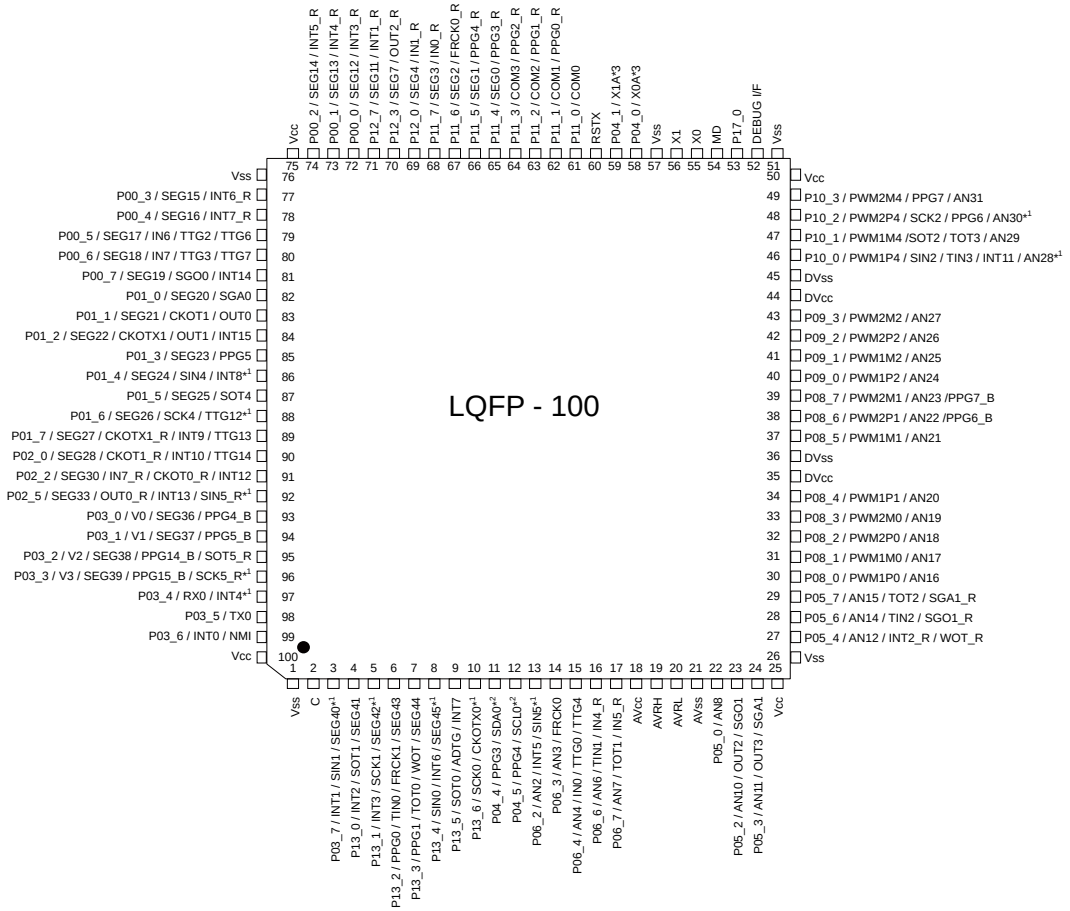
・These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

BLOCK DIAGRAM



PIN ASSIGNMENTS

(TOP VIEW)



(FPT-100P-M20)

*1: CMOS input level only
*2: CMOS input level only for I^2C
*3: Please set Rom Configuration Block (RCB) to use the subclock
All other general-purpose pins have only Automotive input level.

PIN FUNCTION DESCRIPTION

Pin name	Feature	Description
ADTG	ADC	A/D converter trigger input
ANn	ADC	A/D converter channel n input
AVcc	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AVss	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
COMn	LCD	LCD Common driver
DVcc	Supply	SMC pins power supply
DVss	Supply	SMC pins power supply
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input
Pnn_m	GPIO	General purpose I/O
OUTn	OCU	Output Compare Unit n waveform output
OUTn_R	OCU	Relocated Output Compare Unit n waveform output
PPGn	PPG	Programmable Pulse Generator n output (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output (8bit)
PWMn	SMC	SMC PWM high current output
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I^2C	I^2C interface n clock I/O input/output
SDAn	I^2C	I^2C interface n serial data I/O input/output
SEGn	LCD	LCD Segment driver
SGAn	Sound Generator	SG amplitude output
SGAn_R	Sound Generator	Relocated SG amplitude output
SGOn	Sound Generator	SG sound/tone output
SGOn_R	Sound Generator	Relocated SG sound/tone output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output

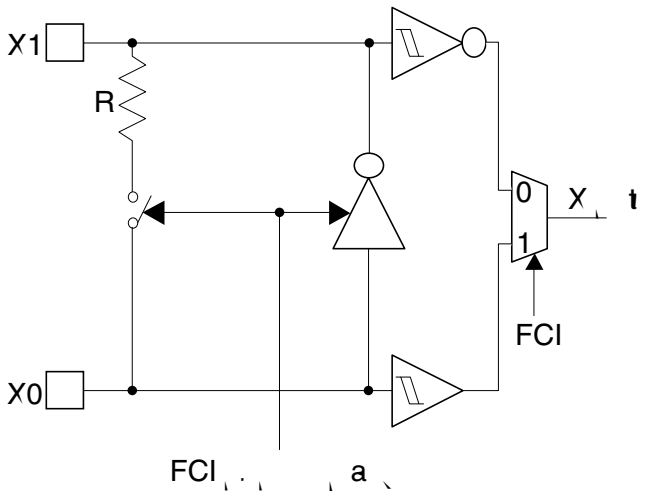
Pin name	Function	Description
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
Vn	LCD	LCD voltage reference
Vcc	Supply	Power supply
Vss	Supply	Power supply
WOT	RTC	Real Time clock output
WOT_R	RTC	Relocated Real Time clock output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output
DEBUG I/F	OCD	On Chip Debugger input/output

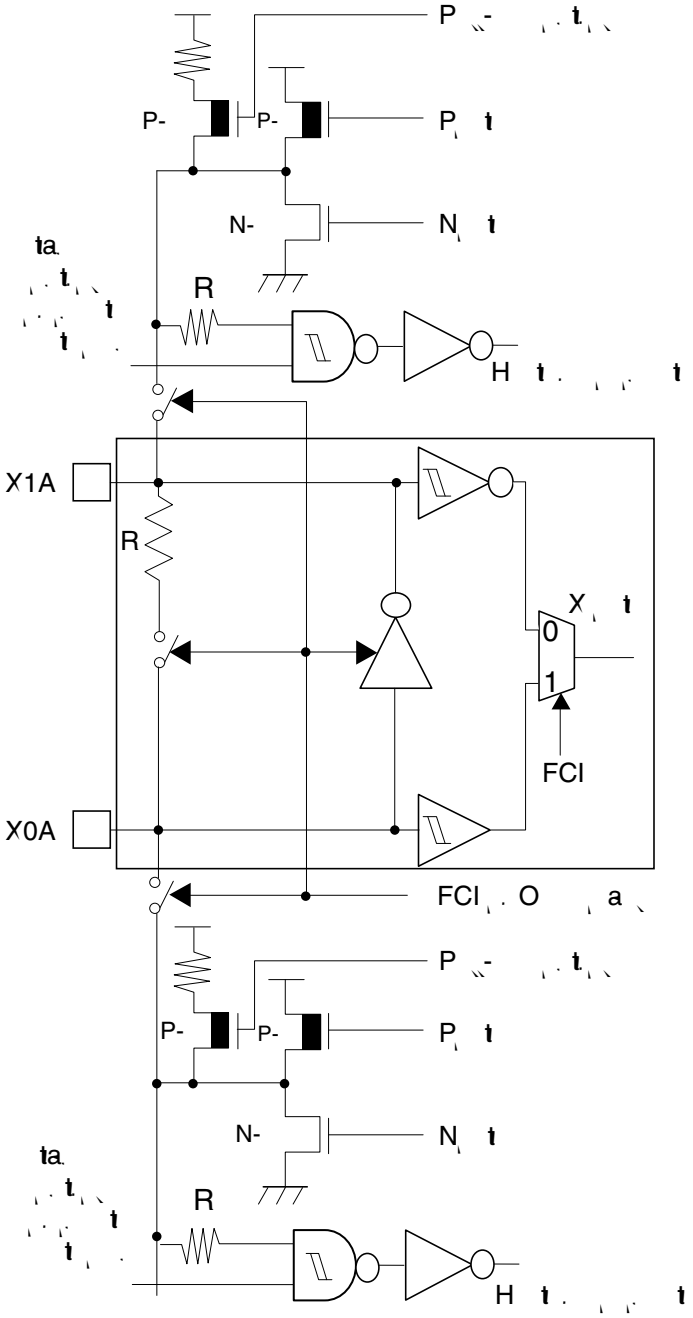
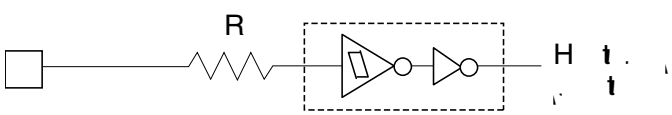
PIN CIRCUIT TYPE

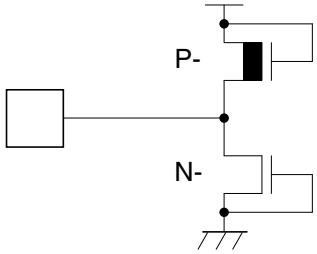
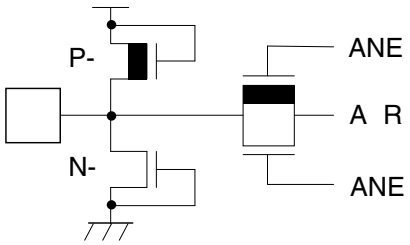
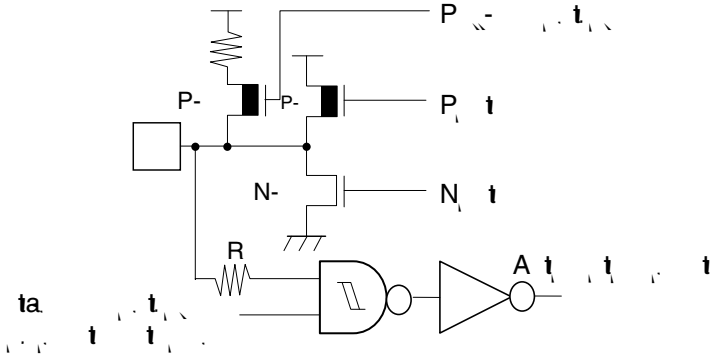
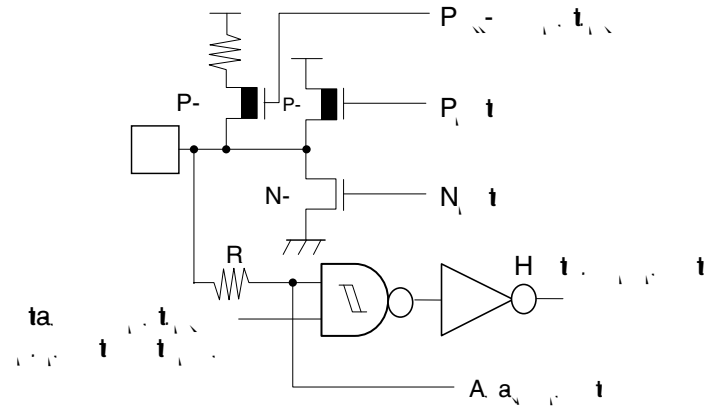
P . . .	I/O . tt *	P . a
1	Supply	Vss
2	F	C
3	P	P03_7 / INT1 / SIN1 / SEG40
4	J	P13_0 / INT2 / SOT1 / SEG41
5	P	P13_1 / INT3 / SCK1 / SEG42
6	J	P13_2 / PPG0 / TIN0 / FRCK1 / SEG43
7	J	P13_3 / PPG1 / TOT0 / WOT / SEG44
8	P	P13_4 / SIN0 / INT6 / SEG45
9	H	P13_5 / SOT0 / ADTG / INT7
10	M	P13_6 / SCK0 / CKOTX0
11	N	P04_4 / PPG3 / SDA0
12	N	P04_5 / PPG4 / SCL0
13	I	P06_2 / AN2 / INT5 / SIN5
14	K	P06_3 / AN3 / FRCK0
15	K	P06_4 / AN4 / IN0 / TTG0 / TTG4
16	K	P06_6 / AN6 / TIN1 / IN4_R
17	K	P06_7 / AN7 / TOT1 / IN5_R
18	Supply	AVcc
19	G	AVRH
20	G	AVRL
21	Supply	AVss
22	K	P05_0 / AN8
23	K	P05_2 / AN10 / OUT2 / SGO1
24	K	P05_3 / AN11 / OUT3 / SGA1
25	Supply	Vcc
26	Supply	Vss
27	K	P05_4 / AN12 / INT2_R / WOT_R
28	K	P05_6 / AN14 / TIN2 / SGO1_R
29	K	P05_7 / AN15 / TOT2 / SGA1_R
30	R	P08_0 / PWM1P0 / AN16
31	R	P08_1 / PWM1M0 / AN17
32	R	P08_2 / PWM2P0 / AN18
33	R	P08_3 / PWM2M0 / AN19
34	R	P08_4 / PWM1P1 / AN20
35	Supply	DVcc

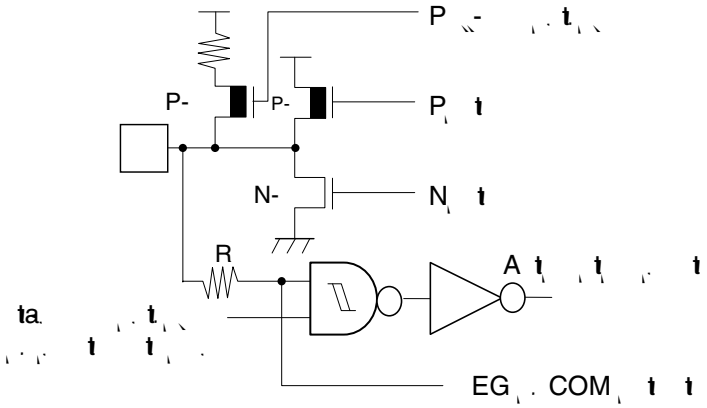
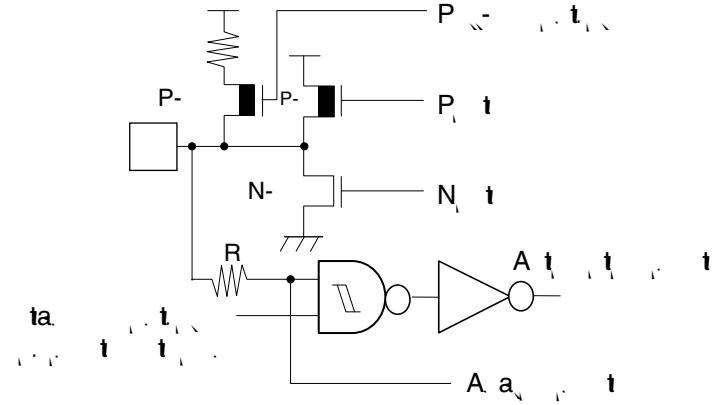
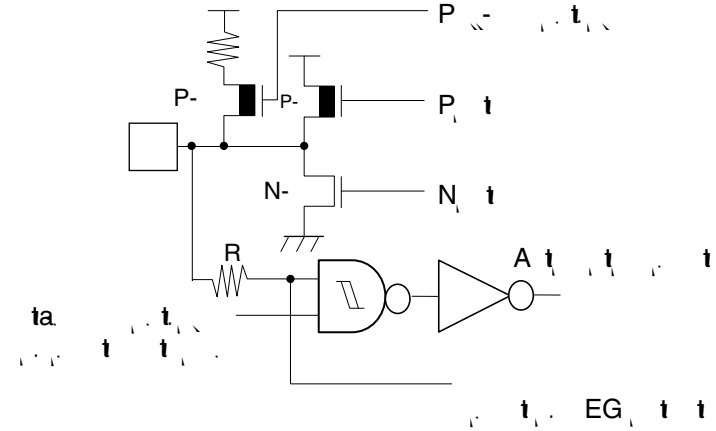
P . .	I/O . tt *	P . a
36	Supply	DVss
37	R	P08_5 / PWM1M1 / AN21
38	R	P08_6 / PWM2P1 / AN22 / PPG6_B
39	R	P08_7 / PWM2M1 / AN23 / PPG7_B
40	R	P09_0 / PWM1P2 / AN24
41	R	P09_1 / PWM1M2 / AN25
42	R	P09_2 / PWM2P2 / AN26
43	R	P09_3 / PWM2M2 / AN27
44	Supply	DVcc
45	Supply	DVss
46	S	P10_0 / PWM1P4 / SIN2 / TIN3 / INT11 / AN28
47	R	P10_1 / PWM1M4 / SOT2 / TOT3 / AN29
48	S	P10_2 / PWM2P4 / SCK2 / PPG6 / AN30
49	R	P10_3 / PWM2M4 / PPG7 / AN31
50	Supply	Vcc
51	Supply	Vss
52	O	DEBUG I/F
53	H	P17_0
54	C	MD
55	A	X0
56	A	X1
57	Supply	Vss
58	B	P04_0 / X0A
59	B	P04_1 / X1A
60	C	RSTX
61	J	P11_0 / COM0
62	J	P11_1 / COM1 / PPG0_R
63	J	P11_2 / COM2 / PPG1_R
64	J	P11_3 / COM3 / PPG2_R
65	J	P11_4 / SEG0 / PPG3_R
66	J	P11_5 / SEG1 / PPG4_R
67	J	P11_6 / SEG2 / FRCK0_R
68	J	P11_7 / SEG3 / IN0_R
69	J	P12_0 / SEG4 / IN1_R
70	J	P12_3 / SEG7 / OUT2_R

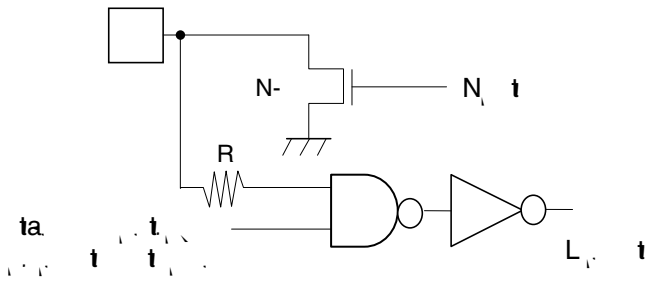
I/O CIRCUIT TYPE

	C. t	R a.
A		High-speed oscillation circuit: · Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) · Feedback resistor = approx. 1.0 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode · The amplitude: 1.8V±0.15V to operate by the internal supply voltage

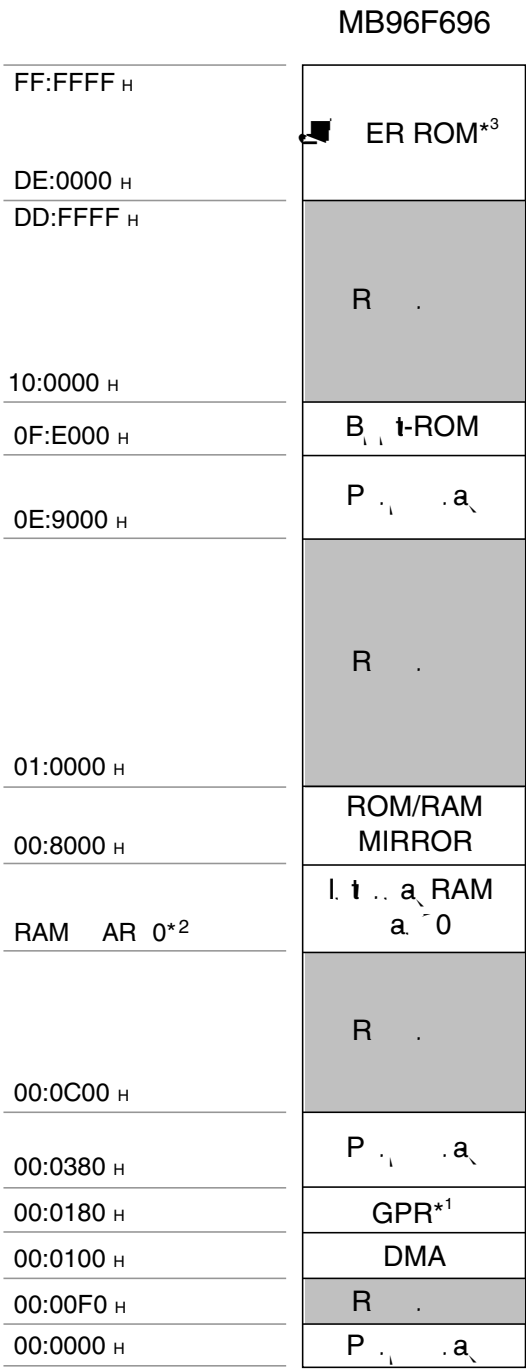
	C. t	R a.
B		Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled • GPIO functionality selectable (CMOS hysteresis input with input shutdown function, I_{OL} = 4mA, I_{OH} = -4mA, Programmable pull-up resistor)
C		• CMOS hysteresis input pin

	C. t	R a.
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Without protection circuit against V_{CC} for pins AVRH
H		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor
I		· CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) · CMOS hysteresis input with input shutdown function · Programmable pull-up resistor • Analog input

	C. t	R a.
J		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • SEG or COM output
K		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
L		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Vx input or SEG output

	C. t	R a.
M		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor
N	———	• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.
O		• I_{OL}: 25mA @ 2.7V • TTL input

MEMORY MAP

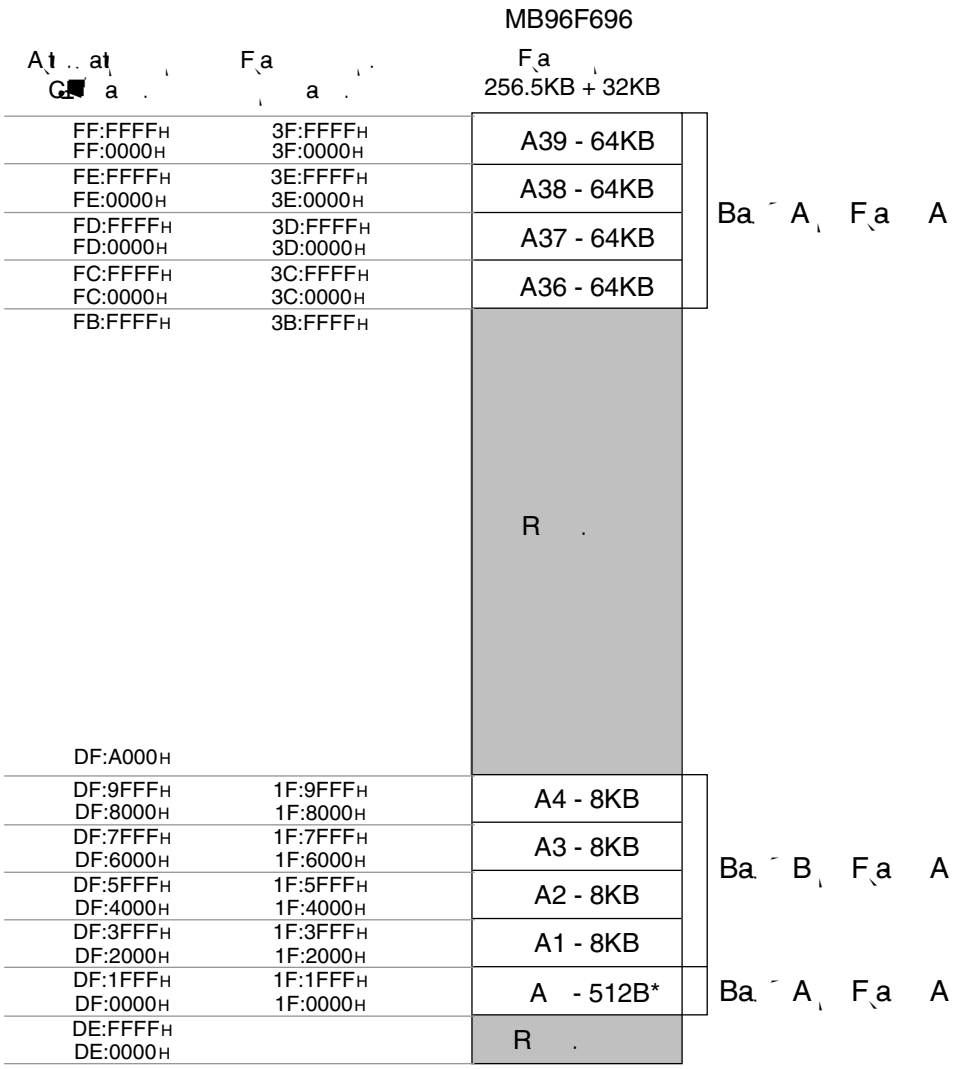


*1: For details about USER ROM area, see the "■USER ROM MEMORY MAP FOR FLASH DEVICES" on the following pages.
*2: For RAMSTART/END addresses, please refer to the table on the next page.
*3: Unused GPR banks can be used as RAM area.

RAMSTART ADDRESSES

D	Ba 0 RAM	RAM AR 0
MB96F696	16KByte	$00:4200_H$

USER ROM MEMORY MAP FOR FLASH DEVICES



*: Phiysical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) are all ROM Mirror area for SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^2PROM emulation.

SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96F696

INTERRUPT VECTOR TABLE

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC	CALLV0	No	-	Reserved
1	3F8	CALLV1	No	-	Reserved
2	3F4	CALLV2	No	-	Reserved
3	3F0	CALLV3	No	-	Reserved
4	3EC	CALLV4	No	-	Reserved
5	3E8	CALLV5	No	-	Reserved
6	3E4	CALLV6	No	-	Reserved
7	3E0	CALLV7	No	-	Reserved
8	3DC	RESET	No	-	Reserved
9	3D8	INT9	No	-	Reserved
10	3D4	EXCEPTION	No	-	Reserved
11	3D0	NMI	No	-	Non-Maskable Interrupt
12	3CC	DLY	No	12	Delayed Interrupt
13	3C8	RC_TIMER	No	13	RC clock timer
14	3C4	MC_TIMER	No	14	Main Clock Timer
15	3C0	SC_TIMER	No	15	Sub Clock Timer
16	3BC	LVDI	No	16	Low Voltage Detector
17	3B8	EXTINT0	Yes	17	External Interrupt 0
18	3B4	EXTINT1	Yes	18	External Interrupt 1
19	3B0	EXTINT2	Yes	19	External Interrupt 2
20	3AC	EXTINT3	Yes	20	External Interrupt 3
21	3A8	EXTINT4	Yes	21	External Interrupt 4
22	3A4	EXTINT5	Yes	22	External Interrupt 5
23	3A0	EXTINT6	Yes	23	External Interrupt 6
24	39C	EXTINT7	Yes	24	External Interrupt 7
25	398	EXTINT8	Yes	25	External Interrupt 8
26	394	EXTINT9	Yes	26	External Interrupt 9
27	390	EXTINT10	Yes	27	External Interrupt 10
28	38C	EXTINT11	Yes	28	External Interrupt 11
29	388	EXTINT12	Yes	29	External Interrupt 12
30	384	EXTINT13	Yes	30	External Interrupt 13
31	380	EXTINT14	Yes	31	External Interrupt 14
32	37C	EXTINT15	Yes	32	External Interrupt 15
33	378	CAN0	No	33	CAN Controller 0
34	374	-	-	34	Reserved
35	370	-	-	35	Reserved
36	36C	-	-	36	Reserved
37	368	-	-	37	Reserved
38	364	PPG0	Yes	38	Programmable Pulse Generator 0
39	360	PPG1	Yes	39	Programmable Pulse Generator 1
40	35C	PPG2	Yes	40	Programmable Pulse Generator 2

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
41	358	PPG3	Yes	41	Programmable Pulse Generator 3
42	354	PPG4	Yes	42	Programmable Pulse Generator 4
43	350	PPG5	Yes	43	Programmable Pulse Generator 5
44	34C	PPG6	Yes	44	Programmable Pulse Generator 6
45	348	PPG7	Yes	45	Programmable Pulse Generator 7

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	2B8	-	-	81	Reserved
82	2B4	-	-	82	Reserved
83	2B0	-	-	83	Reserved
84	2AC	-	-	84	Reserved
85	2A8	-	-	85	Reserved
86	2A4	-	-	86	Reserved
87	2A0	-	-	87	Reserved
88	29C	-	-	88	Reserved
89	298	FRT0	Yes	89	Free Running Timer 0
90	294	FRT1	Yes	90	Free Running Timer 1
91	290	-	-	91	Reserved
92	28C	-	-	92	Reserved
93	288	RTC0	No	93	Real Time Clock
94	284	CAL0	No	94	Clock Calibration Unit
95	280	SG0	No	95	Sound Generator 0
96	27C	IIC0	Yes	96	I^2C interface0
97	278	-	-	97	Reserved
98	274	ADC0	Yes	98	A/D Converter
99	270	-	-	99	Reserved
100	26C	-	-	100	Reserved
101	268	LINR0	Yes	101	LIN USART 0 RX
102	264	LINT0	Yes	102	LIN USART 0 TX
103	260	LINR1	Yes	103	LIN USART 1 RX
104	25C	LINT1	Yes	104	LIN USART 1 TX
105	258	LINR2	Yes	105	LIN USART 2 RX
106	254	LINT2	Yes	106	LIN USART 2 TX
107	250	-	-	107	Reserved
108	24C	-	-	108	Reserved
109	248	LINR4	Yes	109	LIN USART 4 RX
110	244	LINT4	Yes	110	LIN USART 4 TX
111	240	LINR5	Yes	111	LIN USART 5 RX
112	23C	LINT5	Yes	112	LIN USART 5 TX
113	238	-	-	113	Reserved
114	234	-	-	114	Reserved
115	230	-	-	115	Reserved
116	22C	-	-	116	Reserved
117	228	-	-	117	Reserved
118	224	-	-	118	Reserved
119	220	-	-	119	Reserved
120	21C	-	-	120	Reserved

HANDLING DEVICES

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication

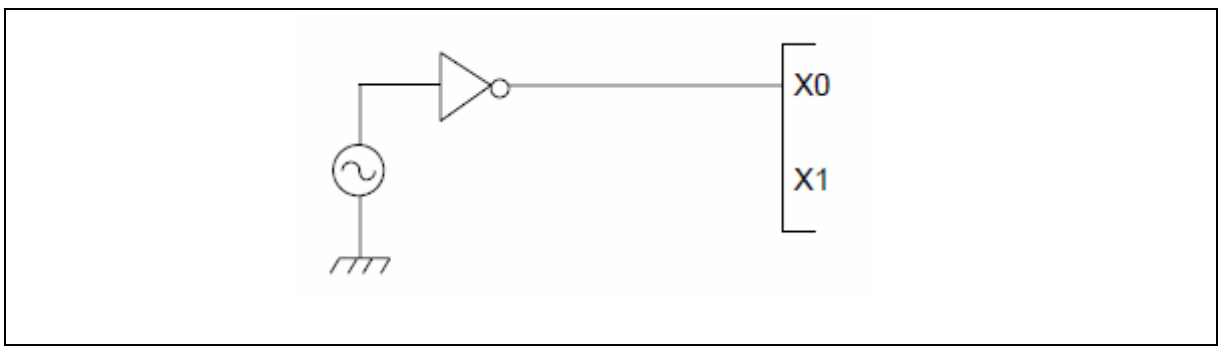
CMOS IC chips may suffer latch-up under the following conditions:
- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.
For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).
Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

The permitted frequency range of an external clock depends on the oscillator type and configuration.
See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

- When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open. And supply 1.8V power to the external clock.



- When using a single phase external clock for the Sub oscillator, ‘External clock mode’ must be selected and X0A/GP04_0 must be driven. X1A/GP04_1 must be configured as GPIO.

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.
V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.
As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between Vcc and Vss as close as possible to Vcc and Vss pins.

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.
It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.
It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.
It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$ $AV_{SS} = AVRH = AVRL = V_{SS}$.

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 Hz to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

All DV_{CC} /DV_{SS} pins must be set to the same level as the V_{CC} /V_{SS} pins.
However note that the SMC I/O pin state is undefined if DV_{CC} is powered on and V_{CC} is below 3V. To avoid this, we recommend to always power V_{CC} before DV_{CC}.

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*[1]	Vcc	-	Vss - 0.3	Vss + 6.0	V	
Analog power supply voltage*[1]	AVcc	-	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc*[2]
Analog reference voltage*[1]	AVRH, AVRL	-	Vss - 0.3	Vss + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, AVRH > AVRL, $AVRL \geq AV_{SS}$
SMC Power supply*[1]	DVcc	-	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc= DVcc*[2]
LCD power supply voltage*[1]	V0 to V3	-	Vss - 0.3	Vss + 6.0	V	V0 to V3 must not exceed Vcc
Input voltage*[1]	V_I	-	Vss - 0.3	Vss + 6.0	V	$V_I \leq (D)V_{CC} + 0.3V$*[3]
Output voltage*[1]	V_O	-	Vss - 0.3	Vss + 6.0	V	$V_O \leq (D)V_{CC} + 0.3V$*[4]

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power consumption*5	P_D	T_A=+105°C	-	333 *6	mW	
Operating ambient temperature	T_A	-	-40	105	°C	
Storage temperature	T_{STG}	-	-55	150	°C	

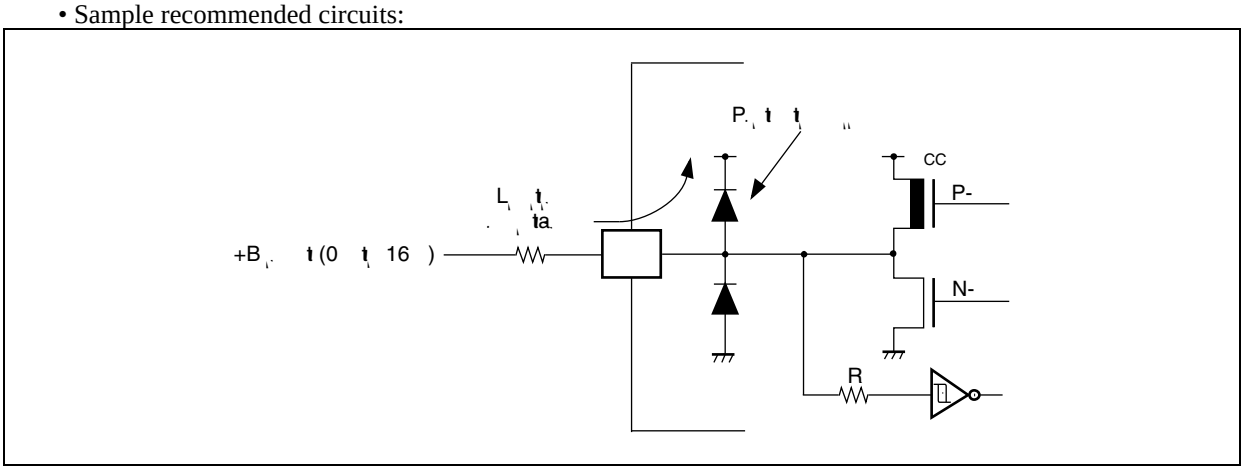
*1: This parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0V$.

*2: AV_{CC}, DV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*4: • Applicable to all general purpose I/O pins (Pnn_m).
• Use within recommended operating conditions.
• Use at DC voltage (current).
• The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
• The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
• Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
• Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

• Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	Vcc, DVcc	2.7	-	5.5	V	
Smoothing capacitor at C pin	Cs	0.5	1.0	1.5	µF	(Target value) 1.0µF (Allowance within ± 50%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than Cs.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

1. Current rating of MB96F696 (Target value)

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes*1	I_{CCPLL}		PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	28.5	-	mA	T_A = +25°C
				-	-	38	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	-	5	-	mA	T_A = +25°C
				-	-	10	mA	T_A = +105°C
	I_{CCSUB}		T 0.0014 Tw 1.252 -1 Td(C)Tj0.0007 Tc 6.51 0 0 6z8.48 08 3d(C n)B = CL5P1/2 = 05Hz (CLK15, CLKSC and	-	0.5	-	mA	T_A = +25°C

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes*2	$I_{CCTMAIN}$	Vcc	Main Timer mode with CLKMC = 4MHz (CLKPLL, CLKRC and CLKSC stopped)	-	285	355	µA	T_A = +25°C
				-	-	1320	µA	T_A = +105°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz	-	160	245	µA	T_A = +25°C
				-	-	1230	µA	T_A = +105°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz	-	35	105	µA	T_A = +25°C
				-	-	1030	µA	T_A = +105°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	90	µA	T_A = +25°C
				-	-	1000	µA	T_A = +105°C
Power supply current in Stop mode*3	I_{CCH}		-	-	20	90	µA	T_A = +25°C
				-	-	1000	µA	T_A = +105°C
Power supply current for active Low Voltage detector*4	I_{CCLVD}		Low voltage detector enabled	-	5	15	µA	
Flash Write/ Erase current*5	$I_{CCFLASH}$		-	-	12.5	20	mA	

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode. The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

*4: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

2. Pin characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC} × 0.7	-	V_{CC} + 0.3	V	CMOS Hysteresis input
			-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "oscillation mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "oscillation mode"	Vcc × 0.8	-	Vcc + 0.3	V	
	V_{IHR}	RSTX	-	Vcc × 0.8	-	Vcc + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	Vcc - 0.3	-	Vcc + 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	Vcc + 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	Vss - 0.3	-	V_{CC} × 0.3	V	CMOS Hysteresis input
			-	Vss - 0.3	-	V_{CC} × 0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "oscillation mode"	Vss	-	VD × 0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "oscillation mode"	Vss - 0.3	-	Vcc × 0.2	V	
	V_{ILR}	RSTX	-	Vss - 0.3	-	V_{CC} × 0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	Vss - 0.3	-	Vss + 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	Vss - 0.3	-	0.8	V	TTL Input

4.5V ≤ Vcc ≤ 5.5V

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage*	V_{OL4}	4mA type	$4.5V \le Vcc \le 5.5V$ $I_{OL} = +4mA$	-	-	0.4	V	
			$2.7V \le Vcc < 4.5V$ $I_{OL} = +1.7mA$					
	V_{OL30}	High Drive type	$4.5V \le Vcc \le 5.5V$ $I_{OL} = +52mA$	-	-	0.5	V	$T_A = -40°C$
			$2.7V \le Vcc < 4.5V$ $I_{OL} = +22mA$					
			$4.5V \le Vcc \le 5.5V$ $I_{OL} = +39mA$					$T_A = +25°C$
			$2.7V \le Vcc < 4.5V$ $I_{OL} = +18mA$					
			$4.5V \le Vcc \le 5.5V$ $I_{OL} = +32mA$					$T_A = +85°C$
			$2.7V \le Vcc < 4.5V$ $I_{OL} = +14mA$					
			$4.5V \le Vcc \le 5.5V$ $I_{OL} = +30mA$					$T_A = +105°C$
			$2.7V \le Vcc < 4.5V$ $I_{OL} = +13.5mA$					
	V_{OL3}	3mA type	$2.7V \le Vcc < 5.5V$ $I_{OL} = +3mA$	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	$Vss < V_I < Vcc$ $AVss, AVRL < V_I < AVcc, AVRH$	- 1	-	1	µA	Single port pin except high current output I/O for SMC
		P08_m, P09_m, P10_m	$DV_{SS} < V_I < DV_{CC}$ $AV_{SS}, AVRL < V_I < AV_{CC}, AVRH$	- 3	-	3	µA	
Total LCD leak current	$\Sigma\|I_{ILCD}\|$	All SEG/ COM pin	Vcc = 5.0V	-	0.5	10	µA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V2, V2 and V1, V1 and V0	Vcc = 5.0V	6.25	12.5	25	kΩ	
Pull-up resistance value	R_{PU}	Pnn_m	Vcc = 5.0V ±10%	25	50	100	kΩ	
Pull-down resistance value	R_{DOWN}	P08_m, P09_m, P10_m	Vcc = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than Vcc, Vss, AVcc, AVss, AVRH, AVRL, P08_m, P09_m, P10_m	-	-	5	15	pF	
		P08_m, P09_m, P10_m	-	-	15	30	pF	

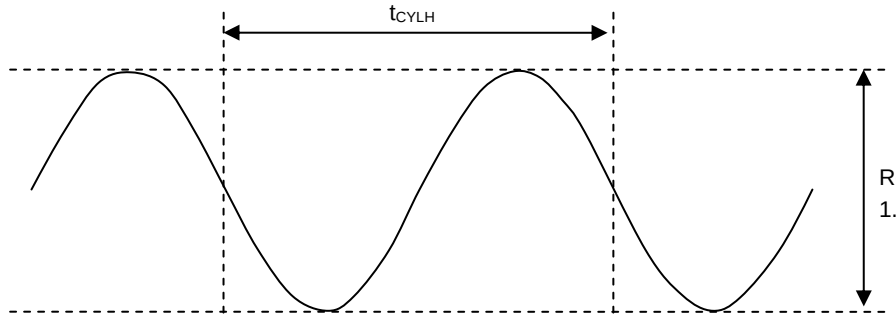
*: I_{OH} and I_{OL} are target value.

4. AC Characteristics

(1) Main Clock Input Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	16	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL off
			4	-	16	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL on
Input clock cycle	t_{CYLH}	-	62.5	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	30	-	70	%	

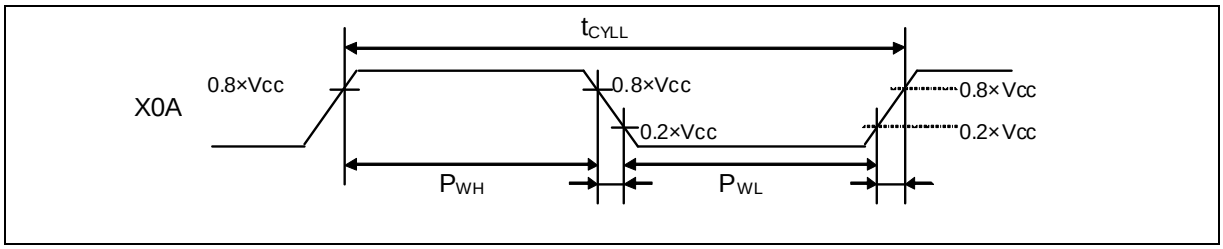


The amplitude changes by resistance, capacity which added outside or the difference of the device.

(2) Sub Clock Input Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min		Max		
Input frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL} P_{WL}/t_{CYLL}	30	-	70	%	



(3) Built-in RC Oscillation Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	F_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator

(4) Internal Clock timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

(5) Operating Conditions of PLL

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	1	-	4	ms	Time from when the PLL starts operating until the oscillation stabilizes
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL macro oscillation clock frequency	f_{PLLO}	56	-	108	MHz	

(6) Reset Input Characteristics

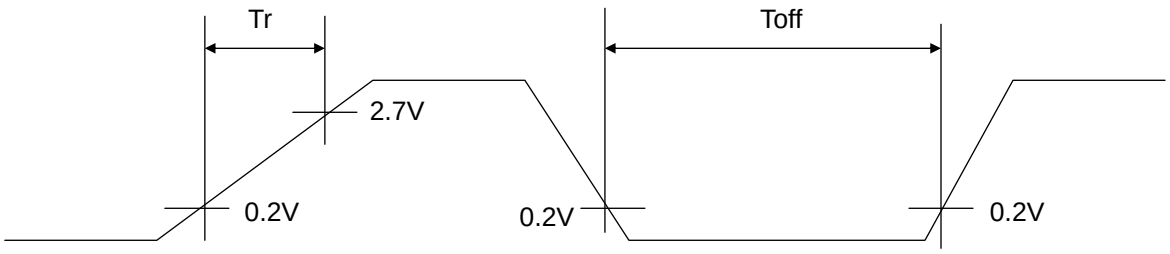
(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	T_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs

(7) Power-on Reset Timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power on rise time	Tr	0.05	-	30	ms
Power off time	Toff	1	-	-	ms



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

(8) USART Timing

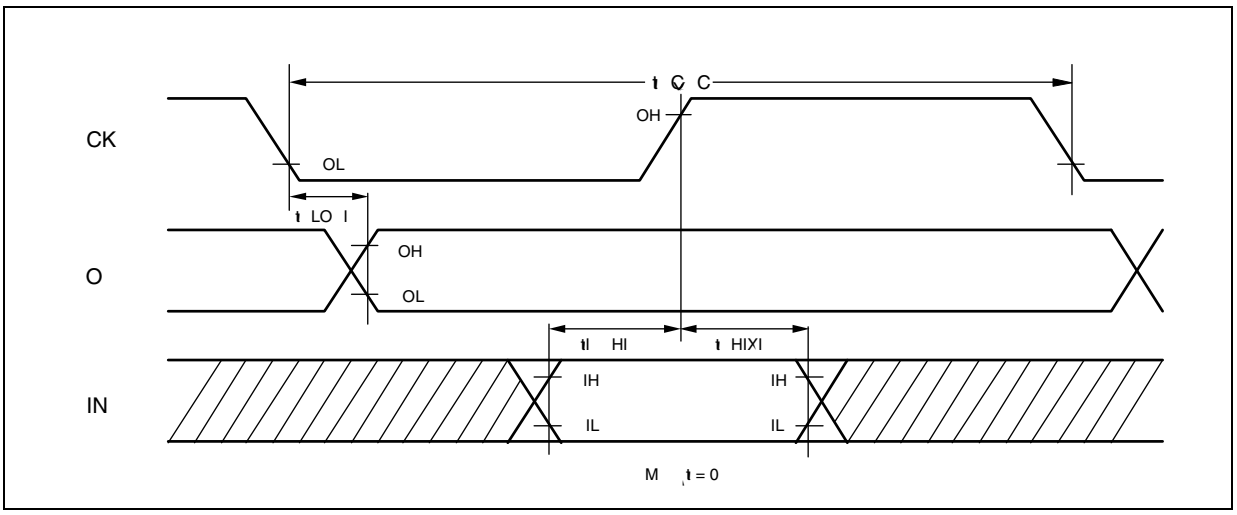
(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

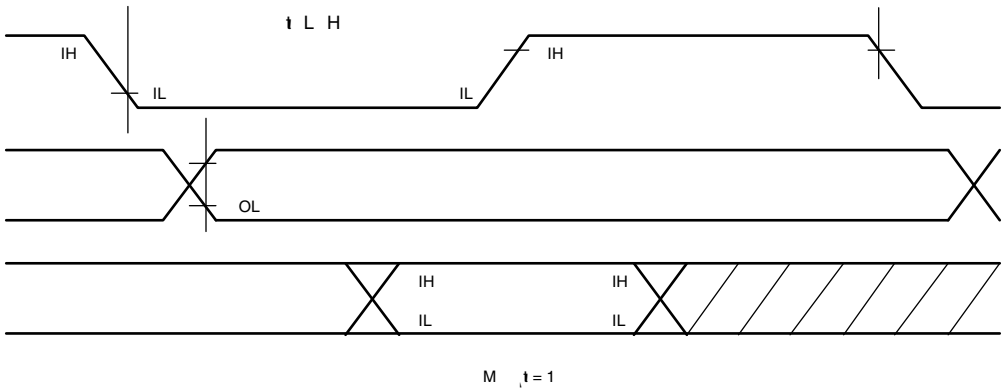
Parameter	Symbol	Pin name	Conditions	4.5V ≤ Vcc < 5.5V		2.7V ≤ Vcc < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	tSCYC	SCKn	Internal shift clock operation	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓ → SOT delay time	tSLOVI	SCKn SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	tOVSHI	SCKn SOTn		N×t_{CLKP1} – 20*	-	N×t_{CLKP1} – 30*	-	ns
SIN → SCK ↑ setup time	tIVSHI	SCKn SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	tSHIXI	SCKn SINn		0	-	0	-	ns
Serial clock "L" pulse width	tSLSH	SCKn	External shift clock operation	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock "H" pulse width	tSHSL	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	tSLOVE	SCKn SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
SIN → SCK ↑ setup time	tIVSHE	SCKn SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK ↑ → SIN hold time	tSHIXE	SCKn SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	tF	SCKn		-	20	-	20	ns
SCK rise time	tR	SCKn		-	20	-	20	ns

Notes:
- The above characteristics apply to CLK synchronous mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96690 series HARDWARE MANUAL”
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKn_0 and SOTn_1 is not guaranteed.

*: Parameter N depends on tSCYC and can be calculated as follows:
• If tSCYC = 2 × k × t_{CLKP1}, then N = k, where k is an integer > 2
• If tSCYC = (2 × k + 1) × t_{CLKP1}, then N = k + 1, where k is an integer > 1
Examples:

tSCYC	N
4 × t_{CLKP1}	2
5 × t_{CLKP1}, 6 × t_{CLKP1}	3
7 × t_{CLKP1}, 8 × t_{CLKP1}	4
...	...


CK
O
IN
OH
OL
IH
IL
M t = 0

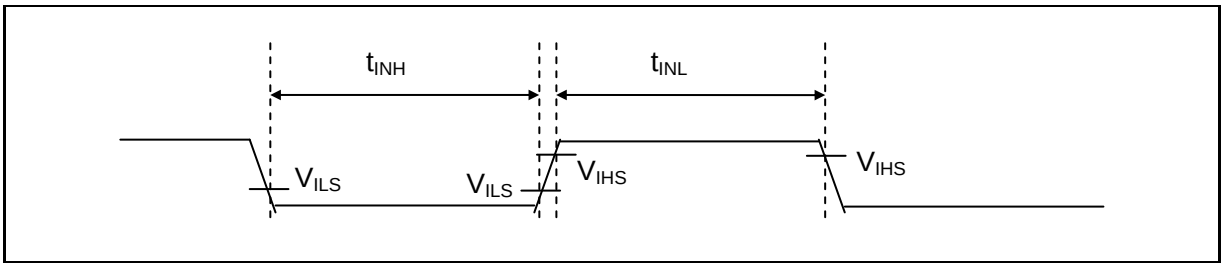

IH
IL
OL
M t = 1

(9) External input timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH} t_{INL}	Pnn_m	$2t_{CLKP1}$ +200 (t_{CLKP1}= $1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG				A/D converter trigger input
		FRCKn, FRCKn_R				Free-Running Timer
		TINn				Reload Timer
		TTGn				PPG Trigger input
		INn, INn_R				Input capture
		INTn, INTn_R, NMI	200	-	ns	External interrupt NMI

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



(10) I^2C timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	fSCL		0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	tHDSTA		4.0	-	0.6	-	µs
SCLclock "L" width	tLOW		4.7	-	1.3	-	µs
SCLclock "H" width	tHIGH		4.0	-	0.6	-	µs
(Repeated) START setup time SCL ↑ → SDA ↓	tSUSTA		4.7	-	0.6	-	µs
Data hold time SCL ↓ → SDA ↓ ↑	tHDDAT		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	tSUDAT→		254Td[(tSUDA)1		006E>TjTf0.604	0	Td(

10bit A/D Converter

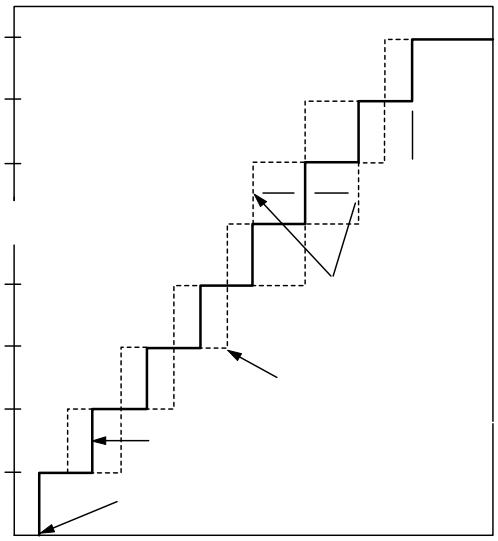
· Electrical characteristics for the A/D converter

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANx	Typ - 20	AVRL + 0.5LSB	Typ + 20	mV	
Full transition voltage	V_{FST}	ANx	Typ - 20	AVRH - 1.5LSB	Typ + 20	mV	
Compare time	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH to AV_{SS})	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	AN 2 to 4, 6 to 8, 10 to 12, 14, 15	-	-	16.0	pF	Normal outputs
		AN 16 to 31	-	-	17.8	pF	High current outputs
Analog port input current	I_{AIN}	AN 2 to 4, 6 to 8, 10 to 12, 14, 15	- 0.3	-	+ 0.3	µA	AV_{SS}, AVRL < V_{AIN} < AV_{CC}, AVRH
		AN 16 to 31	- 3	-	+ 3	µA	
Analog input voltage	V_{AIN}	ANx	AVRL	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS} + 0.1	V	

• Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0b0000000000 ← → 0b0000000001) and the full-scale transition point (0b1111111110 ← → 0b1111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linearity error.

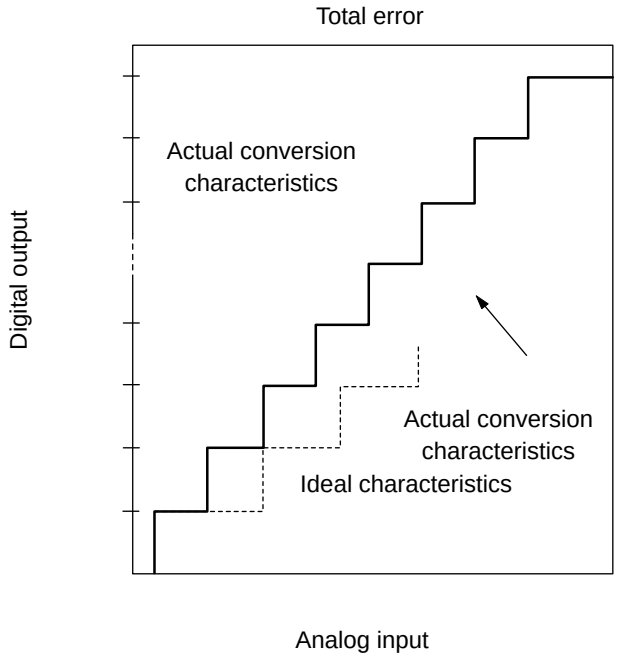


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB'} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.



$$1LSB' \text{ (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1LSB' \times (N - 1) + 0.5LSB'\}}{1LSB'}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT}' (Ideal value) = AVRL + 0.5LSB[V]
V_{FST}' (Ideal value) = AVRH - 1.5LSB[V]

High current output slew rate

(V_{CC} = AV_{CC} = 2.7V to 5.5V, DV_{CC} = 4.5V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Rise time / Fall time	t_{R2}, t_{F2}	P08_m, P09_m, P10_m	15	-	75	ns	C_L=85pF

z

Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

		Value		

ORDERING INFORMATION

Part number	Flash memory	Package
MB96F696RAPMC-GSE1*	Flash A (288.5KB)	100-pin plastic LQFP (FPT-100P-M20)
MB96F696RAPMC-GSE2*		

*: These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

REVISION HISTORY

Revision	Date	Modification

MEMO

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